

## IN THE CLAIMS

1. (Allowed) An integrated circuit comprising:
  - a dielectric layer formed over a substrate;
  - a first damascene structure in the dielectric layer, the first damascene structure comprising a bottom surface and first and second sidewalls;
  - a first conductor located in the damascene structure, the conductor comprising a conductive material having a random grain orientation;
  - a first liner layer lining the bottom surface and sidewalls of the first damascene structure and encapsulating the first conductor by contacting a top surface of the first conductor, wherein the first liner layer imparts the random grain orientation in the conductive material of the first conductor to improve electromigration lifetime of the first conductor;
  - a second damascene structure in the dielectric layer, the second damascene structure comprising a bottom surface and second sidewalls and disposed above said first damascene structure;
  - a second conductor located in the damascene structure, the conductor comprising a conductive material having a random grain orientation;
  - a second liner layer lining the bottom surface and sidewalls of the second damascene structure and encapsulating the second conductor by contacting a top surface of the second conductor, wherein the second liner layer imparts the random grain orientation in the conductive material of the second conductor to improve electromigration lifetime of the second conductor;
  - and
  - wherein said second liner layer is in contact with said first liner layer.

2. (Allowed) An integrated circuit of claim 1, wherein a conductive material of the first and second liners comprises a random grain orientation.

3. (Allowed) An integrated circuit of claim 1, wherein a conductive material of the first and second liners comprises an amorphous character.

4. (Allowed) An integrated circuit of claim 1, wherein a conductive material of the first and second liners is chosen from a group consisting essentially of titanium nitride, tantalum and tantalum nitride.

5. (Allowed) An integrated circuit of claim 4, wherein a conductive material of the first and second liners comprises a random grain orientation or amorphous character.

6. (Withdrawn and Currently Canceled)

7. (Allowed) An integrated circuit of claim 1, wherein the liner comprises a layer of titanium nitride, the layer being between about 10 Angstroms and about 1000 Angstroms thick.

8. (Allowed) An integrated circuit of claim 7, wherein the layer of titanium nitride is about 50 Angstroms thick.

9. (Allowed) An integrated circuit of claim 8, wherein the layer of titanium nitride is a layer of  $N_2/H_2$  plasma treated titanium nitride.

10. (Allowed) An integrated circuit of claim 1, further comprising a subliner.

11. (Allowed) An integrated circuit of claim 10, wherein the subliner is a layer of titanium.

12. (Allowed) An integrated circuit of claim 11, wherein the layer of titanium for the subliner is between about 10 Angstroms and about 300 Angstroms thick.

13. (Allowed) An integrated circuit of claim 1, wherein the conductive materials of the first and second conductors comprise at least one material chosen from the group consisting essentially of aluminum, copper and tungsten.

14. (Allowed) An integrated circuit of claim 13, further comprising a subliner comprising titanium.

15. (Allowed) An integrated circuit of claim of claim 14, wherein the conductor has a thickness of about 3700 Angstroms.

16-27. (Withdrawn and Currently Canceled)

28. (Allowed) An integrated circuit comprising:  
a conductor comprising a conductive material having a random grain orientation, the conductor forming device interconnections having a damascene structure; and  
a liner surrounding at least three surfaces of the conductor, wherein the liner is amorphous and wherein the liner imparts the random grain orientation in the conductive material of the conductor to improve the electromigration lifetime of the conductor.

29. (Allowed) An integrated circuit of claim 28, wherein the conductor is aluminum.

30. (Allowed) An integrated circuit of claim 29, wherein the liner comprises titanium nitride.